REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-7 are presently active in this case. The present amendment cancels Claims 8-29 without prejudice or disclaimer.

In the outstanding Office Action, Claims 1-2 were rejected under 35 U.S.C. §103(a) as unpatentable over Fan et al. (U.S. Patent No. 6,404,222, herein "Fan") in view of Chen (U.S. Patent No. 6,414,498). Claims 3-4 were rejected under 35 U.S.C. §103(a) as unpatentable over Fan in view of Chen and further in view of Oosawa et al. (U.S. Patent No. 6,597,191, herein "Oosawa"). Claim 5 was rejected under 35 U.S.C. §103(a) as unpatentable over Fan in view of Chen and further in view of Fried et al. (U.S. Patent No. 6,624,651, herein "Fried"). Claims 6-7 were indicated as allowable if rewritten in independent form.

Applicants acknowledge with appreciation the indication of allowable subject matter. However, since Applicant considers that Claim 1, from which Claims 6-7 depend, defines patentable subject matter, Claims 6-7 are maintained in dependent form at the present time.

In response to the Restriction Requirement being made final, Claims 8-29, directed to non-elected inventions, are cancelled without prejudice or disclaimer. Applicants reserve the right to present claims directed to the non-elected inventions in a divisional application, which shall be subject to the third sentence of 35 U.S.C. §121.[1]

In response to the rejection of Claims 1-2 under 35 U.S.C. §103(a), Applicants respectfully request reconsideration of this rejection and traverse the rejection, as discussed next.

Briefly recapitulating, Applicants' Claim 1 relates to a capacitance measurement circuit. The circuit includes, *inter alia*: First, second and third terminals, said first terminal

[1] "A patent issuing on an application with respect to which a requirement for restriction under this section has been made ... shall not be used as a reference ... against a divisional application." See also MPEP 804.01.

being accompanied by ***a first capacitance including first and second capacitance components to be measured*** and a non-target capacitance component not to be measured, said third terminal being accompanied by a dummy capacitance having the same capacitance value as said non-target capacitance component; and target capacitance forming section formed between said first terminal and said second terminal so that said first terminal is accompanied by said first capacitance component.

As explained in Applicants' Specification at page 2, lines 2-18, Applicants' invention improves upon background capacitance measurement circuits, since it allows separate measurements of the first and second capacitance components, a precautionary measure that the ***first capacitance component is merely a part of the first capacitance***. Thus, Applicants' invention as recited in Claim 1, wherein the first capacitance accompanying a first terminal includes first and second capacitance components, can be separated into the first and second capacitance components and the non-target capacitance components based on the values of the first to third currents detected with the first to third current detectors, thereby enabling separate measurement of the first and second capacitance components.

Turning now to the applied references, Fan discloses a capacitance measurement circuit, wherein a capacitance of a capacitor within the silicon chip is measured using the difference in average charging current flowing from the measurement circuit via a left and a right capacitor.[2] Fan, however, fails to teach or suggest Applicants' claimed capacitance measurement circuit. In particular, and as acknowledged by the outstanding Office Action,[3] Fan fails to teach or suggest the claimed first capacitance including first and second capacitance components to be measured.

[2] See Fan in the Abstract and in Figures 4-5, reference numerals 408 and 412.
[3] See the outstanding Office Action at page 4, lines 4-6.

The outstanding Office Action rejects Applicants' Claims 1-2 based on the proposition that Chen discloses the above feature[4], and that it would have been obvious to modify Fan by importing this feature from Chen to arrive at Applicants' claimed invention. Applicants respectfully submit, however, that Chen also fails to disclose the above feature related to first capacitance including first and second capacitance components to be measured, as next discussed.

In Chen's circuit shown in Figure 1, target interconnect capacitances c_1-c_N are arranged between wiring 105 and corresponding interconnects 106-1 to 106-N, respectively. Accordingly, every interconnect 106-n ($1 \leq n \leq N$) is accompanied by only one interconnect capacitance c_n. In addition, as clearly seen from Chen's equations (1) and (2),[5] the measurement method of the interconnect capacitances c_n is obtained independently of the remaining interconnect configurations 105 and 106-n. Moreover, Chen explicitly states that "[t]he method just described may be performed similarly for any of the other target interconnect capacitances c_1, ..., c_{n+1}, ..., c_N in the interconnect configuration 104."[6]

Therefore, even if *in arguendo* any of the interconnects 106-1 to 106-N would read to be corresponding to the second terminal of Applicants' Claim 1, only one interconnect capacitance c_n exists between the first terminal (interconnect 105 side) and the second terminal (interconnect 106-n side). More specifically, in Chen, only the interconnect capacitance c_n between the interconnect 105 and the interconnect 106-n is disclosed as a capacitance accompanying the first terminal, and therefore Chen fails to teach or suggest Applicants' claimed two capacitance components.

Accordingly, as explained above, Chen does not disclose a second capacitance component being different from the first capacitance component, of the first and second

[4] See the outstanding Office Action at page 4, lines 7-10.
[5] See Chen at column 7, lines 1-17.
[6] See Chen at column 7, lines 19-22.

capacitance components that are included in the first component accompanying the first terminal, as recited in Applicants' Claim 1.

The remaining references used to form the other 35 U.S.C. §103(a) rejections do not remedy the deficiencies of Fan and Chen. The reference Oosawa discloses a noise absorbing switch, and shows a cross-section thereof in Figure 6. Oosawa's gate electrodes are arranged inside an insulation film.[7] However, Oosawa is silent on any arrangements so as to influence capacitors. The other reference Fried, used to form an obviousness-type rejection of Claim 5, does not remedy the deficiencies of Fan, Chen and Oosawa. Accordingly, even if we assume *in arguendo* that the combination of the applied reference Fan, Chen, Oosawa and Fried is proper, the combination fails to teach or suggest the feature regarding the first and second capacitance components, as recited in Claim 1.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-7 is earnestly solicited.

[7] See Oosawa in Figure 6.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,

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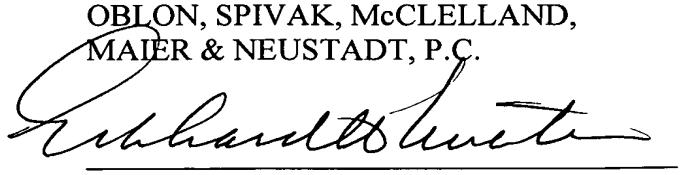

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